Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A device for breakinga leakage current path in a memory array within a memory device, comprising:
a column selection line adapted to select a column of a memory cell within a memory array;
a row selection line adapted to select a row of the memory cell within the memory array; and
a switch device coupled to the memory cell, a power supply terminal, the column selection line and the row selection line, wherein when the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, the switch device is turned off so that a power provided from the power supply terminal is not coupled to the memory cell, and when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell.

[c2] 2. The device for breaking the leakage current path of claim 1, wherein the switch device further comprises:
a first switch coupled to the memory cell, the power

supply terminal and the column selection line, wherein when the column selection line receives the column turn-off signal, the first switch is turned off so that the power is not coupled to the memory cell, and when the column selection line does not receive the column turn-off signal, the power is coupled to the memory cell; and a second switch coupled to the memory cell, the power supply terminal and the row selection line, wherein when the row selection line receives the row turn-off signal, the second switch is turned off so that the power is not coupled to the memory cell, and when the row selection line does not receive the row turn-off signal, the power is coupled to the memory cell.

[c3] 3. The device for breaking the leakage current path of claim 2, wherein each of the first switch and the second switch comprises a PMOS transistor or PMOSFET transistor.

[c4] 4. The device for breaking the leakage current path of claim 1, wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal.

[c5] 5. A method for breaking a leakage current path for a circuit having an array, the method comprising:
selecting a column in response to a memory cell within a memory array;

selecting a row in response to the memory cell within the memory array; and

coupling a column turn-off signal to the column and a line turn-off signal to the row so that a power provided from a power supply terminal is not coupled to the memory cell, wherein when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell.

[c6] 6. The method for breaking the leakage current path of claim 5, wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal.

[c7] 7. A memory device, comprising:

a column selection line adapted to select a column of a memory cell within a memory array;

a row selection line adapted to select a row of the memory cell within the memory array; and

a device for breaking a leakage current path comprising a switch device coupled to the memory cell, a power supply terminal, the column selection line and the row selection line, wherein when the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, the switch device is turned off so that a power provided from the power sup-

ply terminal is not coupled to the memory cell, and when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell.

[c8] 8. The memory device of claim 7, wherein the switch device further comprises:
a first switch coupled to the memory cell, the power supply terminal and the column selection line, wherein when the column selection line receives the column turn-off signal, the first switch is turned off so that the power is not coupled to the memory cell, and when the column selection line does not receive the column turn-off signal, the power is coupled to the memory cell; and
a second switch coupled to the memory cell, the power supply terminal and the row selection line, wherein when the row selection line receives the row turn-off signal, the second switch is turned off so that the power is not coupled to the memory cell, and when the row selection line does not receive the row turn-off signal, the power is coupled to the memory cell.

[c9] 9. The memory device of claim 8, wherein each of the first switch and the second switch comprises a PMOS transistor or PMOSFET transistor.

[c10] 10. The memory device of claim 7, wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal.

[c11] 11. The memory device of claim 7, wherein the memory array comprises a DRAM array.